KL-300
Digital Logic Lab

The KL-300 Digital Logic Lab is a comprehensive and self-contained system suitable for anyone engaged in digital logic experiments.

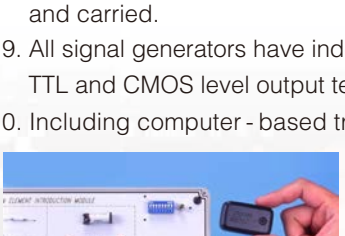
All the necessary equipment for digital logic experiments such as power supply, signal generator, switches and displays are installed on the main unit.

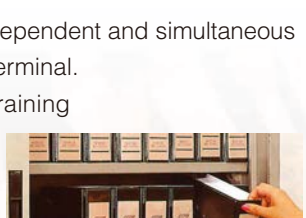
The 13 modules cover a large variety of essential topics for digital logic. It is a time and cost saver for both students and engineers interested in developing and testing circuit prototypes.

+ Simulation

● Features

1. Suitable for combination logic, sequential logic and microprocessor circuits design and experiments.
2. Ideal tool for learning the basics of digital logic circuits.
3. Comprehensive power, signal supply and testing devices for convenient experiments.
4. Experiments are expandible and flexible with universal breadboard.
5. Capable of processing TTL, CMOS, NMOS, PMOS and ECL circuits.
6. All supply units are equipped with overload protection for safety purpose.
7. All modules equipped with 8-bit DIP switch for fault simulations.
8. Individual storage cases for all modules to be easy kept and carried.
9. All signal generators have independent and simultaneous TTL and CMOS level output terminal.
10. Including computer - based training





● Specifications

Main Unit (KL-31001)

1. Dual DC Power Supply
   (1) Voltage range : +5V/1.5A, -5V/0.3A, ±12V/0.3A
   (2) With output overload protection
2. Adjustable DC Power Supply
   (1) Voltage range : +1.5V~+15V
   (2) Maximum current output : 0.5A
   (3) With output overload protection
3. Standard Frequency
   (1) Frequency : 1MHz, 60Hz, 1Hz
   (2) Accuracy : ±0.01% (1MHz)
   (3) Fan out : 10 TTL load
4. Clock Signal Generator
   (1) Frequency : 1Hz ~1MHz (6 ranges)
   a. 1Hz ~ 10Hz d. 1KHz ~ 10KHz
   b. 10Hz ~ 100Hz e. 10KHz ~ 100KHz
   c. 100Hz ~ 1KHz f. 100KHz ~ 1MHz
   (2) Fan out : 10 TTL load
5. Data Switch
   (1) 8-bit DIP switch x 2, 16-bit TTL level output
   (2) Toggle switch x 4, each with Debounce circuit
   (3) Fan out : 10 TTL load

6. Pulser Switch
   (1) 2 sets of independent control output
   (2) Each set with Q, $\overline{Q}$ output, pulse width > 5ms
   (3) Each set of switch with Debounce circuit
   (4) Fan out : 10 TTL load

7. Line Signal Generator
   (1) Frequency : 50Hz/60Hz
   (2) Output voltage : 6Vrms
   (3) With overload protection

8. Thumbwheel Switch
   2-digit, BCD code output and common point input

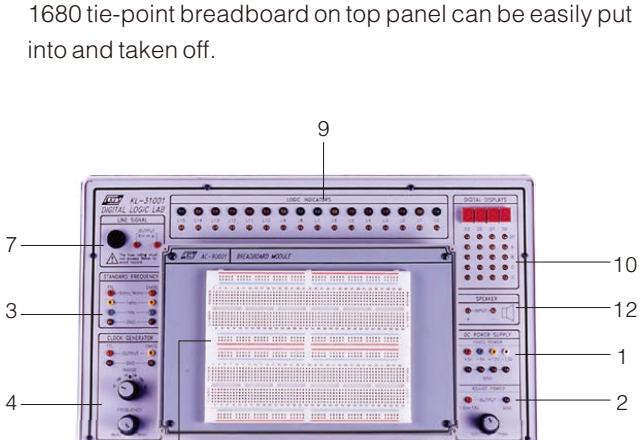
9. Logic Indicator
   (1) 16 sets of independent LED indicates high and low logic state
   (2) Input Impedance : ≥100KΩ

10. Digital Displays
   (1) 4 sets of independent 7-segment LED display
   (2) With BCD, 7-segment decoder/driver and DP input
   (3) Input with 8-4-2-1 code

11. Logic Probe
   (1) TTL and CMOS level
   (2) 5mm LED displays
   (3) "Lo" and "Hi" LED display low/high logic state respectively

12. Speaker
   One 8Ω, 0.25W speaker with driver circuit

13. Breadboard Modules (AC-90001)
   1680 tie-point breadboard on top panel can be easily put into and taken off.

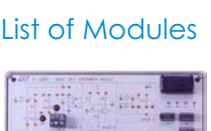


KL-31001

Experiment Modules

1. All 13 modules are equipped with an 8-bit DIP switch for fault simulation. Users learn how to solve various. problems by setting the DIP switch to different positions
2. Solutions for all fault test are listed in the experiment manual for user's reference.
3. 2mm plugs and sockets are used throughout the main unit and all modules.
4. Comprehensive experiment manual and instructor's manual
5. Module dimension : 255x165x30mm.
6. Connection plugs are used on the modules to prevent accidental damages.
7. Individual keeping case for each module.

List of Modules



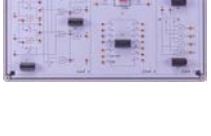
KL-33001
Basic Logic Gates Experiments

KL-33002
Combinational Logic Circuit Experiments(1)

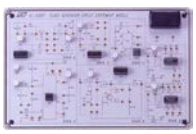
KL-33003
Combinational Logic Circuit Experiments (2)

KL-33004
Combinational Logic Circuit Experiments (3)

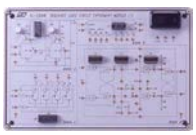
KL-33005
Combinational Logic Circuit Experiments (4)



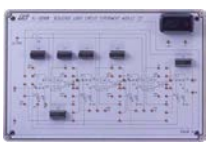
KL-33006
Combinational Logic Circuit Experiments (5)



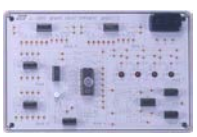
KL-33007
Clock Generator Circuit Experiments



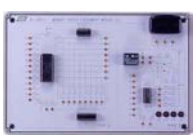
KL-33008
Sequential Logic Circuit Experiments (1)



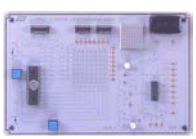
KL-33009
Sequential Logic Circuit Experiments (2)



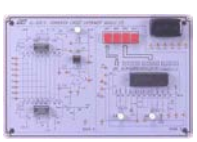
KL-33010
Memory Circuit Experiments (1)



KL-33011
Memory Circuit Experiments (2)



KL-33012
Converter Circuit Experiments (1)



KL-33013
Converter Circuit Experiments (2)

List of Experiments

1. Basic Logic Gates Experiments
   - 1-1 Introduction to logic gates and switches.....KL-33001(A)
   - 1-2 Logic gates circuits
     - a. Diode Logic (DL) circuit .....KL-33001(C)
     - b. Resistor-Transistor Logic (RTL) circuit.....KL-33001(B)
     - c. Diode-Transistor Logic (DTL) circuit .....KL-33001(B.C)
     - d. Transistor-Transistor Logic (TTL) circuit.....KL-33001(D)
     - e. CMOS logic circuit.....KL-33001(E)
   - 1-3 Threshold voltage measurement
     - a. TTL threshold voltage measurement .....KL-33001(D)
     - b. CMOS threshold voltage measurement...KL-33001(E)
   - 1-4 Voltage/current measurement
     - a. TTL I/O voltage/current measurement.....KL-33001(D)
     - b. CMOS voltage/current measurement.....KL-33001(E)
   - 1-5 Basic logic gate transmission delay measurement
     - a. TTL gate delay time measurement .....KL-33001(D)
     - b. CMOS gate delay time measurement.....KL-33001(E)
   - 1-6 Measurement of basic logic gates characteristics
     - a. AND gate characteristics measurement .....KL-33001(D)
     - b. OR gate characteristics measurement .....KL-33001(D)
     - c. INVERTER gate characteristics measurement .....KL-33001(D)
     - d. NAND gate characteristics measurement....KL-33001(D)
     - e. NOR gate characteristics measurement.....KL-33001(D)
     - f. XOR gate characteristics measurement.....KL-33001(D)
   - 1-7 Interface between logic gates
     - a. TTL to CMOS interface .....KL-33001(D.E)
     - b. CMOS to TTL interface .....KL-33001(D.E)
2. Combinational Logic Circuits Experiments
   - 2-1 NOR gate circuits .....KL-33002(A)
   - 2-2 NAND gate circuit .....KL-33002(B)
   - 2-3 XOR gate circuit
     - a. Constructing XOR gate with NAND gate .....KL-33002(B)
     - b. Constructing XOR gate with basic gate.....KL-33002(C)
   - 2-4 AND-OR-INVERT (AOI) gate circuit.....KL-33002(C)
   - 2-5 Comparator circuits
     - a. Comparator constructed with basic logic gates .....KL-33002(C)
     - b. Comparator constructed with TTL IC .....KL-33002(D)
   - 2-6 Schmitt gate circuit .....KL-33002(A)
   - 2-7 Open-collector gate circuits
     - a. High voltage/current circuit .....KL-33002(E)
     - b. Constructing an AND gate with open-collector gate .....KL-33002(E)
   - 2-8 Tristate gate circuits
     - a. Truth table measurements.....KL-33003(C)
     - b. Constructing an AND gate with tristate gate .....KL-33003(C)
     - c. Bidirectional transmission circuit.....KL-33003(C)
   - 2-9 Half-adder and full-adder circuits
     - a. Constructing HA with basic logic gates.....KL-33004(A)
     - b. Full adder circuit .....KL-33004(B)
     - c. High-speed adder carry generator circuit.....KL-33003(A)
     - d. BCD code adder circuit .....KL-33004(B)
   - 2-10 Half-subtractor and full-subtractor circuit
     - a. Subtractor circuit constructed with basic logic gates .....KL-33004(A)
     - b. Full adder and inverter circuit .....KL-33004(B)
   - 2-11 Arithmetic Logic Unit (ALU) circuit .....KL-33003(B)
   - 2-12 Bit parity generator circuit
     - a. Bit parity generator constructed with XOR gates .....KL-33004(A)
     - b. Bit parity generator IC .....KL-33003(D)

2-13 Encoder circuit
a. Constructing a 4-to-2 encoder with basic gates .....KL-33005(A)
b. Constructing a 10-to-4 encoder with TTL IC .....KL-33006(A)
2-14 Decoder circuit
a. Constructing a 2-to-4 decoder with basic gates .....KL-33005(C)
b. Constructing a 4-to-10 decoder with TTL IC .....KL-33004(C)
c. BCD to 7-segment decoder .....KL-33005(B)
2-15 Multiplexer circuit
a. Constructing a 2-to-1 multiplexer .....KL-33006(E)
b. Using multiplexers to create functions .....KL-33006(F)
c. Constructing a 8-to-1 multiplexer with TTL IC .....KL-33006(F)
2-16 Demultiplexer circuit
a. Constructing a 2-output demultiplexer .....KL-33006(E)
b. Constructing a 8-output demultiplexer .....KL-33006(B)
2-17 Digitally controlled analog multiplexer/demultiplexer circuit
a. Analog switch characteristics .....KL-33006(C.D)
b. Bidirectional transmission with CMOS IC analog switches .....KL-33006(C)

3. Clock Generator Circuit Experiments
3-1 Constructing oscillator circuit with basic logic gates .....KL-33007(A)
3-2 Constructing oscillator circuit with schmitt gate .....KL-33007(B)
3-3 Voltage controlled oscillator (VCO) circuit .....KL-33007(C)
3-4 555 IC oscillator circuit
a. 555 oscillator circuit .....KL-33007(D)
b. VCO circuit .....KL-33007(D)
3-5 Monostable multivibrator circuits
a. Low-speed monostable multivibrator circuits .....KL-33007(E)
b. High-speed monostable multivibrator circuits .....KL-33007(E)
c. Constructing monostable multivibrator circuits .....KL-33007(D)
d. Constructing non-retriggerable circuit with TTL-IC .....KL-33007(F)
e. Constructing retriggerable circuit with TTL-IC .....KL-33007(G)
f. Constructing a variable duty cycle oscillator circuit with monostable multivibrator .....KL-33008(A)

4. Sequential Logic Circuit Experiments
4-1 Flip-flop circuits
a. Constructing a R-S flip-flop with a basic logic gates .....KL-33008(D)
b. Constructing a D flip-flop with a R-S flip-flop .....KL-33008(D)
c. Constructing a J-K flip-flop with a D flip-flop .....KL-33008(D)
d. Constructing a J-K flip-flop with a R-S flip-flop .....KL-33008(D)
e. Constructing a shift register with a D flip-flop .....KL-33008(C)
f. Preset left/right shift register .....KL-33008(B)
g. Constructing a noise elimination circuit with R-S flip-flop .....KL-33008(D)

4-2 J-K flip-flop circuits
a. Asynchronous binary up-counter .....KL-33009(A)
b. Asynchronous decade up-counter .....KL-33010(D)
c. Asynchronous divide-by-N up-counter .....KL-33010(C)
d. Asynchronous binary down-counter .....KL-33009(A)
e. Synchronous binary up-counter .....KL-33009(A)
f. Synchronous binary up/down counter .....KL-33009(A)
g. Presetable synchronous binary up/down counter .....KL-33010(A)
h. Presetable synchronous decimal up/down counter .....KL-33010(B)
i. Ring counter .....KL-33009(A)
j. Johnson's counter .....KL-33009(A)

5. Memory Circuit Experiments
5-1 Constructing Read Only Memory (ROM) with diodes .....KL-33010(F)
5-2 Constructing Random Access Memory (RAM) with D flip-flop .....KL-33010(G)
5-3 64-bit RAM circuit .....KL-33011(B)
5-4 Erasable Programmable Read Only Memory (EPROM) circuit .....KL-33010(E)
5-5 Electronic EPROM (EEPROM) circuit .....KL-33011(A)
5-6 Constructing dynamic scanning counter with single-chip microprocessor .....KL-33012(A)

6. Converter Circuit Experiment
6-1 Digital/Analog Converter (DAC) circuit
a. Unipolar DAC circuit .....KL-33013(A)
b. Bipolar DAC circuit .....KL-33013(A)
6-2 Analog/Digital Converter (ADC) circuit
a. 8-bit converter circuit .....KL-33012(B)
b. 3 1/2-digit converter circuit .....KL-33013(B)

Accessories(KL-38002)

1. Experiment manual and instructor's manual
2. Connection leads and plugs : 1 set
3. Key : 1 pce

Computer-Based Training

1. Built-in circuit simulation of experiment modules.
2. Fault simulation is allowed.
3. Users can flexibly compare the simulation analysis result with hardware signal output.
4. Support virtual instrument.